

1 of 15 ATTY, DOCKET NO. SERIAL NUMBER PTO-1449 (Modified) 10/037,171 RA001C13 U.S. DEPARTMENT OF COMMERCE APPLICANT(S) PATENT AND TRADEMARK OFFICE FARMWALD ET AL. INFORMATION DISCLOSURE FILING DATE GROUP ART UNIT **STATEMENT** December 21, 2001 2181 BY APPLICANT

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
Ø	5,034,964	Jul. 23, 1991	Khan et al.		1	
M	4,755,937	July 5, 1989.8	Glier	1	1	
M	4,875,192	Oct 17, 1989	Matsumoto	_	-	

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	OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)
M	Hansen et al., "A RISC MICROPROCESSOR WITH INTEGRAL MMU AND CACHE INTERFACE", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 145-148
MA	Moussouris et al., "A CMOS PROCESSOR WITH INTEGRATED SYSTEMS FUNCTIONS", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 126-130
A	"LR2000 High Performance RISC Microprocessor Preliminary" LSI Logic Corp. 1988, pp. 1-15
MA	"LR2010 Floating Point Accelerator Preliminary" LSI Logic Corp. 1988, pp 1-20
184	"High Speed CMOS Databook", Integrated Device Technology Inc. Santa Clara, CA, 1988 pp 9-1 to 9-14
1014	Riordan T. "MIPS R2000 Processor Interface 78-00005(C)", MIPS Computer Systems, Sunnyvale, CA, June 30, 1987, pp 1-83
M	Monssouris, J. "The Advanced Systems Outlook-Life Beyond RISC: The next 30 years in high-performance computing", Computer Letter, July 31, 1989 (an edited excerpt from an address at the fourth annual conference on the Advanced Systems Outlook, in San Francisco, CA (June 5))

examiner Glenn Anve	DATE CONSIDERED $5/12/2093$
EXAMINER: Initial citation if reference was considered. Draw line	through citation if not in conformance to MPEP 609 and not considered.

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		2 of 15	
PTO-1449 (Modified)	ATTY. DOCKET NO. RA001C13	SERIAL NUMBER 10/037,171	
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE December 21, 2001	GROUP ART UNIT 2181	

U.S. PATENT DOCUMENTS FILING NAME **SUB** DATE EXAMINER DOCUMENT CLASS **CLASS** DATE NUMBER INTUALS Redwine et al. May 18, 1982 1/4 4,330,852 James Oct. 27, 1987 4,703,418 Fischer Nov. 15, 1988 4,785,394 4,726,021 Feb. 16, 1988 Horiguchi et al. Sept. 26, 1989 Kimoto et al. 4,870,562

FOREIGN PATENT DOCUMENTS DOCUMENT SUB EXAMINER COUNTRY CLASS CLASS INITIAL NUMBER DATE July 7, 1981 Japan S56-82961 S57-14922 Jan. 26, 1982 Japan Sho 60-80193 May 8, 1983 Japan HA Mar. 30, 1985 Japan Sho 60-55459 S61-72350 April 14, 1986 Japan June 14, 1988 Japan S63-142445 B63-46864 Sept. 19, 1988 Japan S64-29951 Jan. 31, 1989 Japan

Watanabe, T.; "Session XIX: High Density SRAMS"; IEEE International Solid State Circuits Conference pp. 266-267 (1987)

Ohno, C.; "Self-Timed RAM: STRAM"; Fujitsu Sci. TechJ., 24, 4, pp 293-300 (Dec. 1988)

"Fast Packet Bus for Microprocessor Systems with Caches", IBM Technical Disclosure Bulletin, pp.279-282 (Jan 1989)

Gustavson, D. "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb 27-Mar 3, 1989)

James, D.; "Scalable I/O Architecture for Busses"; IEEE, pp. 539-544 (April 1989)

EXAMINER GILINA Aure	DATE CONSIDERED 5/12/2003
EXAMINER: Initial citation if reference was considered. Draw line lockide copy of this form with post communication to applicant.	through citation if not in conformance to MPEP 609 and not considered.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE December 21, 2001	GROUP ART UNIT 2181		

		U.S. PAT	ENT DOCUMENTS			
EXAMINE R INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
An	4,205,373	May 27, 1980	Shah et al.			
M	4,845,670	Jul. 4, 1989	Nishimoto et al.		_	
MA	4,509,142	Apr. 2, 1985	Childers			
120	4,183,095	Jan. 8, 1980	Ward			
MA	4,685,088	Aug. 4, 1987	Ianucci		_	
1911	4,975,872	12/04/90	Zaiki		_	
an	5,016,226	05/14/91	Hiwada et al.		-	

FOREIGN PATENT DOCUMENTS SUB **EXAMINER** DOCUMENT **CLASS** COUNTRY CLASS INITIAL NUMBER DATE April 28, 1987 **EPO** 0 246 767 0 334 552 Mar. 16, 1989 **EPO** EPO 0 276 871 Jan. 29, 1988

European Search Report for EPO Patent Application No. 00 101 1832

European Search Report for EPO Patent Application No. 89 30 2613

Z. Amitai, "New System Architectures for DRAM Control and Error Correction", Monolithic Memories Inc., Electro/87 and Mini/Mico Northeast: Focusing on the OEM Conference Record, pp. 1132, 4/31-3, (April 1987)

N. Siddique, "100-MHz DRAM Controller Sparks Multiprocessor Designs", Electronic Design, pp. 138-141, (Sept 1986)

H. Kuriyama et al., "A 4-Mbit CMOS SRAM WITH 8-NS SERIAL ACCESS TIME", IEEE Symposium On VLSI Circuits Digest Of Technical Papers, pp. 51-52, (June 1990)

J. Chun et al., "A 1.2ns GaAs 4K Read Only Memory", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 83-86, (Nov. 1988)

A. Fielder et al., "A 3 NS 1K X 4 STATIC SELF-TIMED GaAs RAM", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 67-70, (Nov. 1988)

JEDEC Standard No. 21C

EXAMINER Glenn Aune	DATE CONSIDERED 5/12/2013
	d. Draw line through citation if not in conformance to MPEP 609 and not considered.

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4 of 15 ATTY, DOCKET NO. SERIAL NUMBER PTO-1449 (Modified) RA001C13 10/037,171 U.S. DEPARTMENT OF COMMERCE APPLICANT(S) PATENT AND TRADEMARK OFFICE FARMWALD ET AL. INFORMATION DISCLOSURE **GROUP ART UNIT** FILING DATE STATEMENT December 21, 2001 2181 BY APPLICANT

		U.S. PAT	ENT DOCUMENTS			
EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
M	4,630,193	Dec. 16, 1986	Kris		~	
Do	4,710,904	Dec. 1, 1987	Suzuki			
BA	4,739,502	Apr. 19, 1988	Nozaki		-	•
M	4,905,201	Feb. 27, 1990	Ohira et al.		_	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) European Search Report for! EPO Patent Application No. 00 10 0018 European Search Report for EPO Patent Application No. 00 10 822 M T.L. Jeremiah et. al., "SYNCHRONOUS PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. M Disc. Bul,. Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982) L. R. Metzeger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. M 18 No. 5, pp. 562-567 (Oct. 1983) A. Yuen ct. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989) Pelgrom et al., "A 32-kbit Variable-Length Shift Register for Digital Audio Application", IEEE Journal of Solid-State Circuits, vol. sc-22, no. 3, June 1987, pp 415-422 Grover et al., "Precision Time-Transfer in Transport Networks Using Digital Crossconnect Systems", 124 IEEE Paper 47.2 Globecom, 1988, pp 1544-1548 Gustavson et al., "The Scalable Interface Project (Superbus)" (DRAFT), SCI-22 Aug 88-doc1 pp 1-16, 201 August 22, 1988 Knut Alnes, "SCI: A Proposal for SCI Operation", SCI-10Nov88-doc23, Norsk Data, Oslo, Norway, pp. 1-12, Nov. 10, 1988 Knut Alnes, "SCI: A Proposal for SCI Operation", SCI-6Jan89-doc31, Norsk Data, Oslo, Norway, pp. 1-MA 24, Jan 6, 1989 Bakka et al., "SCI: Logical Level Proposals", SCI-6Jan89-doc32, Norsk Data, Oslo, Norway, pp. 1-20, BA Jan 6, 1989 Knut Alnes, "Scalable Coherent Interface", SCI-Feb 89-doc52, (To appear in the Eurobus Conference M Proceedings May 1989), pp. 1-8 Boysel et al., "Four-Phase LSI Logic Offers New Approach to Computer Designer", Four-Phase Systems Inc. Cupertino, CA, Computer Design, April 1970, pp. 141-146, Boysel et al., "Random Access MOS Memory Packs More Bits To The Chip", Electronics, Feb. 16, M 1970, pp. 109-146,

EXAMINER Gylun Aure	DATE CONSIDERED 5/12/2003
EXAMINER: Initial citation if reference was considered. Draw line Include copy of this form with next communication to applicant.	through citation if not in conformance to MPEP 609 and not considered.

5 of 15 ATTY, DOCKET NO. SERIAL NUMBER PTO-1449 (Modified) RA001C13 10/037,171 U.S. DEPARTMENT OF COMMERCE APPLICANT(S) PATENT AND TRADEMARK OFFICE FARMWALD ET AL. INFORMATION DISCLOSURE GROUP ART UNIT FILING DATE STATEMENT 2181 December 21, 2001 BY APPLICANT

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		<u>U.S. PAT</u>	ENT DOCUMENTS		, 	
EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
M	4,206,833	04/27/93	Lee GOYAR	th -	_	
PAR	4,953,128	· 08/28/90	Kawai et al.		_	
124	5,140,688	08/18/92	White et al.		_	
124	5,018,111	05/21/91	Madland	-	_	
/BA	4,845,664	07/04/89	Aichelmann, Jr. et al.		_	
M	4,734,880	03/29/88	Collins		_	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5-um Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988) T. Williams et. al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", M IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988) D. Jones, "Synchronous static ram", Electronics and Wireless World, vol.93, no.1622, pp. 1243-4 (Dec. 87) F. Miller et. al., "HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMS", /aa Midcon/87 Conference Record, pp. 430-432 Chicago, IL, USA; 15-17 Sept. 1987 K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986) K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990) F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989) M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference D. Wendell et al. "A 3.511s, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990) S. Watanabe et. al., "AN Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial READ/WRITE Mode", IEEE Journal of Solid State Circuits, vol. 24 No. 3, pp. 763-770 (June 1982) K. Numata et. al. "New Nibbled-Page Architecture for High Density DRAM's", IEEE Journal of Solid State Circuits, vol. 24 No. 4, pp. 900-904 (Aug. 1989) H. L. Kalter et al. "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC" IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1118-1128 (Oct 1990) J. Sonntag et al. "A Monolithic CMOS 10MHz DPLL for Burst-Mode Data Retiming", IEEE International Solid State Circuits Conference (ISSCC) February 16, 1990

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EXAMINER	Glenn	Anve	DATE CONSIDERED 5/12/2003	
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6 of 15 ATTY. DOCKET NO. SERIAL NUMBER RA001C13 10/037,171 APPLICANT(S) FARMWALD ET AL. FILING DATE GROUP ART UNIT

INFORMATION DISCLOSURE **STATEMENT** BY APPLICANT

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U.S. DEPARTMENT OF COMMERCE

PATENT AND TRADEMARK OFFICE

December 21, 2001

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: U.S. PATENT DOCUMENTS							
EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE	
BA	4,649,511	03/10/97	Gdula				
<i>C</i> A	4,860,198	08/22/89	Takenaka		_		
1921	3,969,706	07/13/76	Procesting et al.	_			
17 A	4,766,536	08/23/88	Wilson, Jr. et al.			•	
104	4,998,262	03/05/91	Wiggers				
- AA	4,757,473	07/12/88	Kurihara et al.	_	_		
120	4,792,926	12/20/88	Roberts				
184	4,811,202	03/07/89	Schabowski				
BA	5,034,917	07/23/91	Bland et al.				
(dA	5,301,278	04/05/94	Bowater et al.	_			
BR	5,153,856	10/06/92	Takahashi				
BA	4,853,896	08/01/89	Yamaguchi				
8n	4,747,079	05/24/88	Yamaguchi				
120	4,945,516	07/31/90	Kashiyama	_			
BA	4,445,204	04/24/84	Nishiguchi	_			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) M. Horowitz et. al., "MIPS-X: A 20-MIPS Peak 32-bit Microprocessor with On-Chip Cache", IEEE Journal of Solid State Circuits, vol. 22 No. 5, pp. 790-799 (Oct. 1987) R. L. Schmidt, "A memory Control Chip for Formatting Data into Blocks Suitable for Video Coding Applications", IEEE Transactions on Circuits And Systems, vol. 36 No. 10, pp. 1275-1280 (Oct 1989) L. R. Metzeger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. SC-18 No. 5, pp. 561-567 (Oct. 1983) A. L. Yuen, "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Oct. 1989)

EXAMINER	Glenn	Aure	DATE CONSIDERED 5/12/2003
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EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

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PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. SERIAL NUMBER 10/037,171				
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<u> </u>		U.S	S, PATENT DOCUMENTS			
EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TAA	5,051,889	09/24/91	Fung ct al.)	
5,361,277 11/01/94		Grover		^		
181	4,954,987	09/04/90	Auvinen et al.	_	-	
MA	4,570,220	02/11/86	Tetrick et al.			

Heller

Smith et al.

Varadi et al.

Nielsen

Bennett et al.

01/27/81

05/21/85

09/12/72 04/24/90

04/21/81

4,247,817 4,519,034

3,691,534

4,920,486

4,263,650

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) S.K. Kwon et al., "Memory Chip Organizations For Improved Reliability In Virtual Memories", IBM Technical Bulletin vol. 25 No. 6, pp. 2952-2957 (Nov 1982) J. Peterson, "System-Level Concerns Set Performance Gains", High Performance Systems, pp. 71-77 (Sept. N. Margulis, "Single Chip CPU Bases Single Chip System Design", High Performance Systems, pp. 34-44 F.Nart, "Multiple Chips Speed CPU Subsystems", High Performance Systems, pp. 46-55 (Sept. 89) D.T. Wong, "An 11-ns 8Kx18 CMOS Static RAM with 0.5-nm Devices", IEEE Journal of Solid State Circuits, vol. 23, No. 5, pp. 1095-1103 (Oct. 1988) A. Agarwal et al., "An Evaluation of Directory Schemes for Cache Coherence", IEEE, pp. 280-289, 1988

EXAMINER Glann Lynn	DATE CONSIDERED 5/12/2003
	hrough citation if not in conformance to MPEP 609 and not considered.

Ø 010

8 of 15 ATTY, DOCKET NO. SERIAL NUMBER PTO-1449 (Modified) RA001C13 10/037,171 U.S. DEPARTMENT OF COMMERCE APPLICANT(S) PATENT AND TRADEMARK OFFICE FARMWALD ET AL. INFORMATION DISCLOSURE FILING DATE GROUP ART UNIT STATEMENT December 21, 2001 2181 BY APPLICANT

		U.S. 1	PATENT DOCUMENTS		<u> </u>	
EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
MA	4,719,602	01/12/88	Hag et al.		_	
MA	5,023,488	06/11/91	Gunning		_	
18A	4,754,433	06/28/88	Chin et al.			
·BA	3,771,145	11/06/73	Wiener	_	_	
104	5,021,985	06/04/91	Hu et al.		_	
BA.	4,821,226	04/11/89	Christopher et al.	-	_	
da	4,882,712	11/21/89	Ohno et, al.	1 ~		
/BA	4,951,251	08/21/90	Yamaguchi et al.		_	
M	4,928,265	7 18 15130105	Hiquehi Beighe et al.		1	
M	5,107,465	04/21/92	J Fung et al.	_	—	

Point

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) D. Hawley, "Superfast Bus Supports Sophisticated Transactions", High Performance Systems, pp. 90-94 M M. Bazes, A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. SC-18, No. 2, pp. 164-172 (April 1983) D. Wendell et al., "A 3.5ns Solf Timed SRAM", IEEE 1990 Symposium on VLSI Circuits pp. 49-50 J. Chun et al., "A pipelined 650 MHz GaAs 8K ROM with Translation Logic" IEEE 1990 GaAs IC ΔA Symposium, pp 139-142 A. L. Yuen, "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid M State Circuits, vol. 24 No. 1, pp. 57-61 (Oct. 1989) Tomoji Takada et al., "A Video Codec LSI for High-Definition TV Systems with One-Transistor DRAM Line Ba Memories," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1656-1659 (Dec. 1989) Amitai, Z., "Burst Mode Memories Improve Cache Design," WESCON/90 Conference Record, pp. 29-32 (Nov. 1990)

EXAMINER GILINA AUVE	DATE CONSIDERED 5/12/2003
EXAMINER: Initial citation if reference was considered Include copy of this form with next communication to	ed. Draw line through citation if not in conformance to MPEP 609 and not considered.

9 of 15 ATTY, DOCKET NO. SERIAL NUMBER PTO-1449 (Modified) RA001C13 10/037,171 U.S. DEPARTMENT OF COMMERCE APPLICANT(S) PATENT AND TRADEMARK OFFICE FARMWALD ET AL. INFORMATION DISCLOSURE **FILING DATE GROUP ART UNIT** STATEMENT December 21, 2001 2181 BY APPLICANT

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U.S. PATENT DOCUMENTS						
EXAMINER INITIALS	DOCUMENT NUMBER	DATE	DATE NAME		SUB CLASS	FILING DATE
Ma	4,673,735	05/05/87	Novak, et. al		_	
/BA	5,684,753	11/04/97	Hashimoto, ct al		1	
BA	4,322,635	03/30/872	Redwine)	
M	4,916,670	04/10/90	Suzuki et al.		1	
184	5,006,982	04/09/91	Ebersole et al.		-	
M	4,636,986	01/13/87	Pinkham	_	_	·
Bn	4,979,145	12/18/90	Remington et al.		_	
194	5,276,846	01/04/94	Aichelmann Jr., et. al)	
M	4,761,567	Aug. 2, 1988	Walters, Jr. et al.	-)	
10/1	5,101,117	Mar. 31, 1992	Johnson et al.		-	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) Ikeda, Hiroaki et al., "100 MHz Serial Access Architecture for 4MB Field Memory," Symposium of VLSI Circuits, Digest of Technical Papers, pp. 11-12 (Jun. 1990) Takasugi, A. et al., "A DATA TRANSFER ARCHITECTURE FOR FAST MULTI-BIT SERIAL ACCESS MODE DRAM", 11TH European Solid State Circuits Conference, Toulouse France pp. 161-165 (Sep. 1985) Ray Pinkham et al., "A 128Kx8 70-MHz Multiport Video RAM with Auto Register Reload and 8x4 WRITE Feature," IEEE Journal of Solid State Circuits, vol. 23, no. 3, pp. 1133-1139 (Oct. 1988) Graham, Andy et al., "Pipelined static RAM endows cache memories with 1-ns speed", Electronic Design pp. 157-170 (Dec. 1984) Robert J. Lodi et al., "Chip and System Characteristics of a 2048-Bit MNOS-BORAM LSI Circuit," IEEE International Solid-State Circuits Conference, (Feb. 1976) Pinkham, Raymond, "A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video Applications," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 6, pp. 999-1007 (Dec. 1984) Ishimoto, S. et al., "A 256K Dual Port Memory," ISSCC Digest of Technical Papers, p. 38-39 (Feb. 1985) Robert J. Lodi et al., "MNOS-BORAM Memory Characteristics," IEEE Journal of Solid-State Circuits, vol. SC-11, No. 5, pp. 622-631 (Oct. 1976) Dave Bursky, "ADVANCED SELF-TIMED SRAM PARES ACCESS TIME TO 5 NS", Electronic Design, pp. 145-147 (Feb. 22, 1990)

EXAMINER Glena Anne	DATE CONSIDERED 5/12/2003
EXAMINER: Initial citation if reference was	considered. Draw line through citation if not in conformance to MPEP 609 and not considered.

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MA	4,482,999	11/13/84		Japson et al.	<u> </u>		Ī	
MA	5,029,124	07/02/91		Leaby et al.	T_		i	
100	5,193,193	03/09/93		Iyer	T	_		
M	4,926,385	05/15/90		Fujishima et al.	T_			
PA	4,566,099	01/21/86		Magerl	T			
BA	4,803,621	02/07/89		Kelly				
100	4,589,108	05/13/86		Billy				
M	4,870,622	09/26/89		Aria et al.				
bn	4,878,166	10/31/89		Johnson et al.				
KIA	4,849,965	07/18/89		Chomel et al.				
04	4,851,990	07/25/89		Johnson et al.				
		FORE	GN PATE	NT DOCUMENTS				
EXAMINER INITIAL	DOCUMENT NUMBER	DATE		COUNTRY	CLASS	SUB CLASS	ZHART EY	SLATIEN S/NO
DA.	sho 58-31637A	Feb 24, 1983	3	Japan	-	<u> </u>		
800	sho 59-165285A	Mar. 11, 1983	3	Japan				
184	sho 60-261095A	June 6, 1984		Japan		i7		
AN	sho 63-300310	Dec. 7, 1988		Japan				
do	hei 2-8950	Jan. 12, 1990		Japan				
M	sho 58-184626A	Oct 28, 1983	,	Japan				
AN_	0 276 871	03/08/8	88	EPO				
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		u.s.	PATENT DOCUMENTS				
EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE	
BO	4,528,661	07/09/85	Bahr et al.				
<i>A</i> 0	4,048,673	09/13/77	Hendric et al.		-		
10A	4,748,617	05/31/88	Drewlo		-		
LOA	4,839,801	06/13/89	Nicely et al.	-	_		
Ab	4,949,301	08/14/90	Joshi et al.		_		
100	3,950,735	04/13/76	Patel	_	_		
Mu	4,047,246	09/06/77	Kerllenevich ct al.		-		
M	4,763,249	08/09/88	Bomba et al.	_	_		
BN	4,625,307	11/25/86	Tulpule et al.	_	_		
		FOREI	GN PATENT DOCUMENTS				
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
M	SHO 58-192154	Nov. 9, 1983	Japan		-		
M	SHO 63-34795	Feb. 15, 1988	Japan]]			
MA	SHO 61-107453	May 26, 1986	Japan				
100	SHO 63-91766	April 22, 1988	Japan_				
do.	SHO 62-16289	Jan. 24, 1987	Japan	1			
M	SHO 61-160556	Oct. 4, 1986	Japan] '	→		
-	OTHER D	OCUMENTS (Inc	cluding Author, Title, Date, Pertinent	Pages, Etc.)			
M. I	Hans-Jurgen Mattaus	ch et al., "A M	emory-Based High-Speed Digita	al Delay Lin	e with a L	arge	
/0kg A	Adjustable Length," Lineback, I Robert	System Spags	f Solid-State Circuits, vol. 23, n Shouldn't Slow the Boom in Fa	st Static RA	Ms," Elec	tronics. DD.	
<i>ON</i> 6	50-62 (July 23, 1997)			45.45.45		
(M) A	Kanopoulos, Nick and Jill H. Hallenbeck, "A First-In, First-Out Memory for Signal Processing Applications," IEEE Transactions on Circuits and Systems, Vol. CAS-33, No. 5, pp. 556-558 (May 1986)					ssing 558 (May	
EXAMINER Glun Alane Date Considered 5/12/2003							

						12 of I	
	PTO-1449 (Modifie	ed)	ATTY. DOCKET NO. RA001C13	SERIA	SERIAL NUMBER 10/037,171		
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		U.S	PATENT DOCUMENTS				
EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE	
<i>/</i> 200	3,691,534	09/12/72	Veradi, et. al		_		
ân	3,771,145	11/06/73	Wiener		-		
M	4,536,795	08/20/85	Hirota, et. al		,		
MA	4,629,909	12/16/86	Cameron		_		
104	4,631,659	12/23/86	Hayne, et. al	T	1		
ΔÅ	4,858,113	08/15/89	Saccardi				
M	4,499,536	02/12/85	Gemma et al.	_	_		
M	4,648,102	03/03/87	Riso, et. al	_	_		
		FORE	GN PATENT DOCUMENTS				
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YESMO	
A)	EP 0424774	05/02/91	EPO	4	7		
1000	EP 0449052	03/29/90	EPO				
	OTHER	DOCUMENTS (In	cluding Author, Title, Date, Pertinent	Pages, Etc.)			
-dn	Takasugi, A. et al., "	A Data-Transfe	r Architecture for Fast Multi-Bit rence, Toulouse, France pp.161-	Serial Aces	Mode DE	RAM," 11 th	
			Charge Addressed Memory," IE			ate Circuits.	
M	Vol. SC-11, No. 5, p	p. 631-636 (Oct	. 1976)				
1/0	Schmitt-Landsiedel, Doris, "Pipeline Architecture for Fast CMOS Buffer RAMs," IEEE Journal of Solid-State Circuits, Vol. 25, No. 3, pp. 741-747 (Jun. 1990)					urnal of	
EXAMINE	Glenn Ann	L	DATE CONSIDERED 3	2/2003			
EXAMINER Include copy	t Initial citation if reference of this form with next com	was considered. D	rnw line through citation if not in conformant.	mance to MPEF	609 and not	considered.	

							13 of 1		
PTO-1449 (Modified):			ATTY. DOCKI		SERIA	SERIAL NUMBER 10/037,171			
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		U.S.	PATENT DOCUM	ENTS					
<u>EXAMINER</u> INITIALS	DOCUMENT NUMBER	DATE	N	AME	CLASS	SUB CLASS	FILING DATE		
700	4,825,287	04/25/89	Baji	, et. al	_	-			
MA	4,845,677	07/04/89	Chapp	ell, et. al	-	-			
m	4,873,671	10/10/89	Kowsl	nik, et. al	T -	_			
Ma	4,876,670	10/24/89	Nakabay	ashi, et. al		-			
M	5,179,667	01/12/1993	I	yer					
<i>O</i> A	4,901,036	02/13/90	Hero	ld, et. al		_			
An	4,970,418	. 11/13/90	Mas	terson	_	-			
M	5,210,715	05/11/93	Но	uston		-			
10A	4,928,265	05/22/90	Higue	hi et al.		_			
KDA	4,953,130	08/28/90	Но	uston		_			
ON	5,251,309	10/05/93	Kinosl	nita et al.		_			
M	4,099,231	07/01/78	Koto	k et al.		_			
		FOREIG	ON PATENT DOCU	JMENTS					
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	CÓUN	ITRY	CLASS	SUB CLASS	TRANSLATION YES/NO		
√ 014	EP 0218523	05/30/89	EP	0	-	7			
MA	JP-A-1-236494	09/21/89	ונ	P					
//2A	Sho 62-71428	03/27/87	Jì	?	1/				
M	EP 0282735	09/21/88	ÉP	0					
	OTHER	DOCUMENTS (Inc	luding Author, Title	e, Date, Pertinent	Pages, Etc.)				
<i>1</i> 5A	1989 GaAs IC Data	Book & Designe	rs Guide, Gigabi	t Logic Inc. (A	ug 1989)				
Mr	"IC's for Entertainme	ent Electronics, F	ricture in Picture	System Edition	n 8.89", Sien	nens AG,	2/89		
EXAMINER	Glenn And	u	DATE CO	NSIDERED 5	1,2/200	>			
EXAMINER Include copy	: Initial citation if reference of this form with next com	was considered. Dr munication to applic	aw line through citati ant.	on if not in confort	nunce to MPEF	609 and not	considered.		

								14 of 15	
			ATT	Y. DOCKET NO. RA001C13	SERIA	SERIAL NUMBER 10/037,171			
	PARTMENT OF CO AND TRADEMAN	1	APP	APPLICANT(S) FARMWALD ET AL.					
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE		NAME	CLASS	SUB CLASS	1	ING ATE	
,DA	5,099,481	04/24/92		Miller				.,	
M	5,016,226	05/14/91		Hiwada, et. al		_			
/ZA	5,023,835	06/11/91		Akimoto, et. al					
· MA	5,036,495	07/30/91		Busch, et. al		_			
BA	5,111,486	05/05/92		Oliboni, et. al		_	•		
1914	5,123,100	06/16/92		Hisada, et. al		_			
FOREIGN PATENT DOCUMENTS									
EXAMINER INITIAL	DOCUMENT NUMBER	DATÉ		COUNTRY	CLASS	SUB CLASS	TRANSI YES	LATION LATION	
M	WO 89/12936	12/28/89		PCT		_			
M	JP 62-51509	03/06/87		Japan					
	OTHER DOCK	JMENTS (Incl	uding .	Author, Title, Date, Pert	inent Pages	s, Etc.)			
	ensson, Christer, "Hi mposium on Circuits			to Chip Communications 8-2231 (Jun. 1991)	Circuit," II	EEE Intern	ational	l	
Wa Wa	akayama, Myles, "A	30-MHz Low-J	litter H	igh-Linearity CMOS Volt		led Oscilla	ator," I	EEE	
				Io. 6, pp. 1074-1081 (Dec I RAMs Build Fast Writal		Stores." E	lectron	ic	
'/A De	sign, pp. 93-96 (Aug	gust 25, 1988)							
/() A Sta	te Circuits, vol. SC-	21, no. 5, pp. 72	20-726						
On So	lid-State Circuits Co	nference Digest	t (Feb.						
1 <i>//</i> 100 1 100 1	i, Jich-Tsorng, "A 10 l. 23, No. 6, pp. 137			OS Comparator," IEEE J	oumal of Sc	olid-State (Circuits 	š,	
/M Mo	otorola MC88200 Ca	che/Memory M	lanager	nent Unit User's Manual,	Motorola In	c. 1989			
	Ramakrishna et al., ' ade-offs" Computer]			ental Supercomputer Des -35	ign Philosop	hies, Deci	isions,	and	
<u> </u>		<u> </u>		7	1				
EXAMINER	Glenn An	ve		DATE CONSIDERED 5/1	42003				
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										15 of 1
	PTO-1449 (Modifie	;d)		ATT	Y.	DOCKET NO. RA001C13	SERIA	L NUMBE 10/037,1		
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			U.S. P	ATEN	T	DOCUMENTS				
EXAMINE INITIALS			DATE			NAME	CLASS	SUB CLASS	FILII DAT	
DA	4,933,953	事	un. 12, 1990	,	T,	Yagi		_		<u></u>
Mp	5,133,064	+	ul. 21, 1992		T	Hotta et al	+-	-		
MA	5,184,027	F	eb. 2, 1993			Masuda et al.	1-	-		
		1	FOREIG	N PAT	E)	NT DOCUMENTS				
EXAMINE INITIAL			DAT			COUNTRY	CLASS	SUB CLASS	TRANSLA' YES/N	TTON 40
<i>P</i> A	JP 1284132	\uparrow	Nov 15,			Japan	·		-	
MA	EP 0 329 418 A	2	Aug 23,	•		EPO		$\overline{/}$		<u> </u>
M	JP 1043894	I	Feb. 16,	, 1989		Japan		1		
	OTHER DOC	 J M [ENTS (Incl	uding /	Αu	thor, Title, Date, Perti	nent Page	s, Etc.)		
<i>79</i> 0	T					poration, Santa Clara, C				
100	"MIPS R3010 copro	- 1	•							
1m	l (pp.1-26, and 60-68))	-			nual", Intel Corporation,			rch 197	2,
MA	"Bipolar/MOS Memo (pp. 4-143 to 4-163)	orie	s Data Book	c", Advi	an	ced Micro Devices, Sun	nyvale, CA	, 1986		
ΔA			tabook", Fuj	itsu Inc	.,	1986 (pp. 1-102 to 1-12	8)			
/0A	"MIPS Chip Set Imp Vol. 3: No. 12; Dec			CL CPU	J*	Microprocessor Report,	MicroDesi	ign Resour	ces Inc.	"
/ 0 M	"R6000 System Bus 22, 1989	& F	R6020 SBC S			tion" MIPS Computer S				
MA	R.A. Volz et al., "PC 1989 – doc-59, pp. 1	l-9				OBAL CLOCK FOR T				
1014	"ECL bus controller No. 1; Pg. 12, Jan. 2			s/s" Mic	cro	oprocessor Report, Micr	oDesign Re	esources In	10., Vol.	. 4:
		극			_					
EXAMINE	R Colens Am				_	DATE CONSIDERED 5/12	2/2007			
	R: Initial citation if reference				thr	ough citation if not in conform	ance to MPEF	2 609 and not	. considere	cd.

PTO/SB/08A (10-01)
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U.S. PATENT DOCUMENTS									
	Cite No.1	Occument Number Number-Kind Code ² (If known	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear				
-BA_		∪\$- 4,823,321	Apr. 18, 1989	Aoyama					
	<u> </u>	US-							
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	FOREIGN PATENT DOCUMENTS										
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PTO-1449 (Modified)	ATTY. DOCKET NO. SERIAL NUMBER 10/037,171			
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.			
INFORMATION DISCLOSURE				
STATEMENT	FILING DATE	GROUP ART UNIT		

December 21, 2001

U.S. PATENT DOCUMENTS

U.S. PATENT DOCUMENTS								
EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE		
M	4,922,141	May 1, 1990	Lofgren et al.	_	ſ			
M	4,253,147	Feb. 24, 1981	MacDougall et al.		j			
m	6,345,321	Feb. 5, 2002	Litaize et al.	REC	EIAE	ED.		
				OCT	3 0 200	2		
				Technolog	y Cente	r 2100		

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
MA	0 329 418	Aug. 23, 1989	United Kingdom	-			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

M	Ralston, E.D. Reilly, "Encyclopedia of Computer Science", Chapman & Hall, 1983, page 1471
M	S.A. Ward, R.H. Halstead, "Computation Structures", The MIT Press, McGraw-Hill Book Company, 1990, pages, 174-175, 93, 250-251, and 258-259
M	Betty Prince, "Semiconductor Memories", Second Edition, John Wiley & Sons, 1991, pages 251, 310, 314, 200-201, 467

EXAMINER	Glenn	Aune	DATE CONSIDERED	dul	2003
LIMITALIC	\circ	$\pi u \sim$	DATE CONSIDERED	J(1 - 1	200/

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